characterization of the present claim in view of the prior art cited. In particular, the Examiner states on page 2 that Perrin teaches the bus arbitrator claimed by the present invention. Perrin's "arbiter (ARB)" is not equivalent to the bus arbitrator of the present invention. Perrin teaches a decoding device in which a memory addressing operation is defined which allows the use of an arbiter module capable of controlling memories of both the DRAM-type and SRAM-type, allowing the use of the same modes of communication with modules M1, M2, M3, etc. (col. 2, ll. 7-12). Perrin's arbiter effects a processing operation on the address bus as a function of the type of connected DRAM memory (col. 4, ll. 48-51).

The bus arbitrator of the present invention arbitrates access to the local bus between the graphics processing circuit and the audio processing circuit (page 3, ll. 11-13). The bus arbitration circuit taught by the present invention monitors the system bus for commands and addresses from the CPU. When the bus arbitration circuit recognizes the address for either the audio or video processing circuit it retrieves the command from the bus, interprets the command and provides the command to either the audio or graphics circuit as appropriate (Page 4, ll. 11-20).

Perrin's arbiter does not retrieve commands from the system bus and provide the appropriate command to either the audio or graphics circuit. Perrin's arbiter effects a processing operation on the address bus that allows the use of both DRAM and SRAM-type memory. Perrin's arbiter does not interpret the address from the CPU and then communicate with the appropriate audio or graphics circuit. Perrin's arbiter converts the address as necessary to communicate with DRAM or SRAM-type memory.

Clearly, Perrin's arbiter is not equivalent to the arbitrator claimed by the present invention. As such, the applicant believes that Claim 1 is not anticipated by Perrin and is in condition for allowance.

2. Claims 2-4 were rejected under 35 U.S.C. §103(a) as being unpatentable over Perrin (U.S. Pat. No. 5,872,577) in view of Neal et al. (U.S. Patent No. 5,761,462). Claims 2-5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Perrin

(U.S. Pat. No. 5,872,577) in view of Herbert et al. (U.S. Pat. No. 5,752,010). Claims 2-5 are dependent upon Claim 1, which has been shown to be allowable. Since each of Claims 2-5 introduces additional patent subject matter, the Applicant believes that Claims 2-5 are in condition for allowance.

3. Claims 6-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Perrin (U.S. Pat. No. 5,872,577) in view of Herbert et al. (U.S. Pat. No. 5,752,010). The applicant believes that Claims 6-23, while including different limitations than Claim 1, are not obvious in view of the prior art cited for the reasons that distinguish Claim 1 over the cited prior art. As such, the Applicant believes that Claims 6-23 are in condition for allowance.

4. If the Examiner believes that a telephone interview may expedite the prosecution of the Application, the Examiner is invited to contact the below attorney at the indicated telephone number.

Respectfully submitted,

MARKISON & RECKAMP, P.C.

By

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